IN THE CLAIMS

1. (Original) A floating gate transistor, comprising:

a first source/drain region and a second source/drain region separated by a channel region in a substrate;

a floating gate opposing the channel region and separated therefrom by a gate oxide;

a control gate opposing the floating gate; and

wherein the control gate is separated from the floating gate by a low tunnel barrier intergate insulator.

2. (Original) The floating gate transistor of claim 1, wherein the low tunnel barrier intergate insulator includes a metal oxide insulator selected from the group consisting of lead oxide (PbO) and aluminum oxide (Al_2O_3).

3. (Original) The floating gate transistor of claim 1, wherein the low tunnel barrier intergate insulator includes a transition metal oxide.

4. (Original) The floating gate transistor of claim 3, wherein the transition metal oxide is selected from the group consisting of Ta_2O_5, TiO_2, ZrO_2, and Nb_2O_5.

5. (Original) The floating gate transistor of claim 1, wherein the low tunnel barrier intergate insulator includes a Perovskite oxide tunnel barrier.

6. (Original) The floating gate transistor of claim 1, wherein the floating gate includes a polysilicon floating gate having a metal layer formed thereon in contact with the low tunnel barrier intergate insulator.

7. (Currently Amended) The floating gate transistor of claim ~~5~~ 6, wherein the control gate includes a polysilicon control gate having a metal layer formed thereon in contact with the low tunnel barrier intergate insulator.

8. (Original) The floating gate transistor of claim 1, wherein the floating gate transistor includes an n-channel type floating gate transistor.

9. (Original) A vertical non volatile memory cell, comprising:

a first source/drain region formed on a substrate;

a body region including a channel region formed on the first source/drain region;

a second source/drain region formed on the body region;

a floating gate opposing the channel region and separated therefrom by a gate oxide;

a control gate opposing the floating gate; and

wherein the control gate is separated from the floating gate by a low tunnel barrier intergate insulator.

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10. (Currently Amended) The vertical non volatile memory cell of claim ~~8~~ 9, wherein the low tunnel barrier intergate insulator includes a metal oxide insulator selected from the group consisting of PbO, Al_2O_3, Ta_2O_5, TiO_2, ZrO_2, and Nb_2O_5. - niobium

lead aluminum tantalum titanium zirconium

11. (Currently Amended) The vertical non volatile memory cell of claim ~~8~~ 9, wherein the floating gate includes a polysilicon floating gate having a metal layer formed thereon in contact with the low tunnel barrier intergate insulator.

12. (Currently Amended) The vertical non volatile memory cell of claim ~~10~~ 11, wherein the control gate includes a polysilicon control gate having a metal layer formed thereon in contact with the low tunnel barrier intergate insulator.

13. (Currently Amended) The vertical non volatile memory cell of claim ~~8~~ 9, wherein the floating gate includes a vertical floating gate formed alongside of the body region.

14. (Currently Amended) The vertical non volatile memory cell of claim ~~12~~ 13, wherein the control gate includes a vertical control gate formed alongside of the vertical floating gate.

15. (Currently Amended) The vertical non volatile memory cell of claim ~~8~~ 9, wherein the floating gate includes a horizontally oriented floating gate formed alongside of the body region.

16. (Currently Amended) The vertical non volatile memory cell of claim ~~14~~ 15, wherein the control gate includes a horizontally oriented control gate formed above the horizontally oriented floating gate.

17. (Original) A non-volatile memory cell, comprising:

a first source/drain region and a second source/drain region separated by a channel region in a substrate;

a polysilicon floating gate opposing the channel region and separated therefrom by a gate oxide;

a first metal layer formed on the polysilicon floating gate;

a metal oxide intergate insulator formed on the metal layer;

a second metal layer formed on the metal oxide intergate insulator; and

a polysilicon control gate formed on the second metal layer.

18. (Currently Amended) The non-volatile memory cell of claim ~~16~~ 17, wherein first and the second metal layers are lead and the metal oxide intergate insulator is lead oxide (PbO).

19. (Currently Amended) The non-volatile memory cell of claim ~~16~~ 17, wherein the first and second metal layer are aluminum and the metal oxide intergate insulator is aluminum oxide (Al_2O_3).

20. (Currently Amended) The non-volatile memory cell of claim ~~16~~ 17, wherein the first and the second metal layers include transition metal layers and the metal oxide intergate insulator includes a transition metal oxide intergate insulator.

21. (Currently Amended) The non-volatile memory cell of claim ~~19~~ 20, wherein the

transition metal oxide is selected from the group consisting of Ta_2O_5, TiO_2, ZrO_2, and Nb_2O_5.

22. (Currently Amended) The non-volatile memory cell of claim ~~19~~ 20, wherein the metal oxide intergate insulator includes a Perovskite oxide intergate insulator.

23. (Currently Amended) The non-volatile memory cell of claim ~~16~~ 17, wherein the floating gate transistor includes a vertical floating gate transistor.

24. (Original) A flash memory array, comprising:

a number of non-volatile memory cells, wherein each non-volatile memory cell includes:

a first source/drain region and a second source/drain region separated by a channel region;

a floating gate opposing the channel region and separated therefrom by a gate oxide;

a control gate opposing the floating gate; and

wherein the control gate is separated from the floating gate by a low tunnel barrier intergate insulator;

a number of sourcelines coupled to the first source/drain regions along a first selected direction in the flash memory array;

a number of control gate lines coupled to the control gates along a second selected direction in the flash memory array; and

a number of bitlines coupled to the second source/drain regions along a third selected direction in the flash memory array.

25. (Currently Amended) The flash memory array of claim ~~22~~ 24, wherein the low tunnel barrier intergate insulator includes a metal oxide insulator selected from the group consisting of PbO, Al_2O_3, Ta_2O_5, TiO_2, ZrO_2, and Nb_2O_5.

26. (Currently Amended) The flash memory array of claim ~~22~~ 24, wherein the floating gate includes a polysilicon floating gate having a metal layer formed thereon in contact with the low

tunnel barrier intergate insulator.

27. (Currently Amended) The flash memory array of claim ~~22~~ 24, wherein the control gate includes a polysilicon control gate having a metal layer formed thereon in contact with the low tunnel barrier intergate insulator.

28. (Currently Amended) The flash memory array of claim ~~22~~ 24, wherein the second selected direction and the third selected direction are parallel to one another and orthogonal to the first selected direction, and wherein the number of control gate lines serve as address lines.

29. (Currently Amended) The flash memory array of claim ~~22~~ 24, wherein the first selected direction and the third selected direction are parallel to one another and orthogonal to the second selected direction, and wherein the number of control gate lines serve as address lines.

30. (Currently Amended) The flash memory array of claim ~~22~~ 24, wherein the first selected direction and the second selected direction are parallel to one another and orthogonal to the third selected direction, and wherein the number of bitlines serve as address lines.

31. (Original) An array of flash memory cells, comprising:

a number of pillars extending outwardly from a substrate, wherein each pillar includes a first source/drain region, a body region, and a second source/drain region;

a number of floating gates opposing the body regions in the number of pillars and separated therefrom by a gate oxide;

a number of control gates opposing the floating gates;

a number of buried sourcelines disposed below the number of pillars and coupled to the first source/drain regions along a first selected direction in the array of memory cells;

a number of control gate lines formed integrally with the number of control gates along a second selected direction in the array of flash memory cells, wherein the number of control gates are separated from the floating gates by a low tunnel barrier intergate insulator; and

a number of bitlines coupled to the second source/drain regions along a third selected

direction in the array of flash cells.

32. (Currently Amended) The array of flash memory cells of claim ~~29~~ 31, wherein the low tunnel barrier intergate insulator includes a metal oxide insulator selected from the group consisting of PbO_2, Al_2O_3, Ta_2O_5, TiO_2, ZrO_2, and Nb_2O_5.

33. (Currently Amended) The array of flash memory cells of claim ~~29~~ 31, wherein each floating gate includes a polysilicon floating gate having a metal layer formed thereon in contact with the low tunnel barrier intergate insulator.

34. (Currently Amended) The array of flash memory cells of claim ~~29~~ 31, wherein each control gate includes a polysilicon control gate having a metal layer formed thereon in contact with the low tunnel barrier intergate insulator.

35. (Currently Amended) The array of flash memory cells of claim ~~29~~ 31, wherein each floating gate is a vertical floating gate formed in a trench below a top surface of each pillar such that each trench houses a pair of floating gates opposing the body regions in adjacent pillars on opposing sides of the trench.

36. (Currently Amended) The array of flash memory cells of claim ~~33~~ 35, wherein the plurality of control gate lines are formed in the trench below the top surface of the pillar and between the pair of floating gates, wherein each pair of floating gates shares a single control gate line, and wherein each floating gate includes a vertically oriented floating gate having a vertical length of less than 100 nanometers.

37. (Currently Amended) The array of flash memory cells of claim ~~33~~ 35, wherein the plurality of control gate lines are formed in the trench below the top surface of the pillar and between the pair of floating gates such that each trench houses a pair of control gate lines each addressing the floating gates one on opposing sides of the trench respectively, and wherein the pair of control gate lines are separated by an insulator layer.

38. (Currently Amended) The array of flash memory cells of claim ~~33~~ 35, wherein the plurality of control gate lines are disposed vertically above the floating gates, and wherein each pair of floating gates shares a single control gate line.

39. (Currently Amended) The array of flash memory cells of claim ~~33~~ 35, wherein the plurality of control gate lines are disposed vertically above the floating gates, and wherein each one of the pair of floating gates is addressed by an independent one of the plurality of control gate lines.

40. (Currently Amended) The array of flash memory cells of claim ~~29~~ 31, wherein each floating gate is a horizontally oriented floating gate formed in a trench below a top surface of each pillar such that each trench houses a floating gate opposing the body regions in adjacent pillars on opposing sides of the trench, and wherein each horizontally oriented floating gate has a vertical length of less than 100 nanometers opposing the body region of the pillars.

41. (Currently Amended) The array of flash memory cells of claim ~~38~~ 40, wherein the plurality of control gate lines are disposed vertically above the floating gates.

42. (Original) An electronic system, comprising:

a processor; and

a memory device coupled to the processor, wherein the memory device includes an array of flash memory cells, comprising:

a number of pillars extending outwardly from a substrate, wherein each pillar includes a first source/drain region, a body region, and a second source/drain region;

a number of floating gates opposing the body regions in the number of pillars and separated therefrom by a gate oxide;

a number of control gates opposing the floating gates;

a number of buried sourcelines disposed below the number of pillars and coupled

to the first source/drain regions along a first selected direction in the array of memory cells;

a number of control gate lines formed integrally with the number of control gates along a second selected direction in the array of flash memory cells, wherein the number of control gates are separated from the floating gates by a low tunnel barrier intergate insulator; and

a number of bitlines coupled to the second source/drain regions along a third selected direction in the array of flash cells.

43. (Currently Amended) The electronic system of claim ~~40~~ 42, wherein the low tunnel barrier intergate insulator includes a metal oxide insulator selected from the group consisting of PbO, Al_2O_3, Ta_2O_5, TiO_2, ZrO_2, and Nb_2O_5.

44. (Currently Amended) The electronic system of claim ~~40~~ 42, wherein each floating gate includes a polysilicon floating gate having a metal layer formed thereon in contact with the low tunnel barrier intergate insulator.

45. (Currently Amended) The electronic system of claim ~~40~~ 42, wherein each control gate includes a polysilicon control gate having a metal layer formed thereon in contact with the low tunnel barrier intergate insulator.

46. (Currently Amended) The electronic system of claim ~~40~~ 42, wherein each floating gate is a vertical floating gate formed in a trench below a top surface of each pillar such that each trench houses a pair of floating gates opposing the body regions in adjacent pillars on opposing sides of the trench.

47. (Currently Amended) The electronic system of claim ~~44~~ 46, wherein the plurality of control gate lines are formed in the trench below the top surface of the pillar and between the pair of floating gates, wherein each pair of floating gates shares a single control gate line, and wherein each floating gate includes a vertically oriented floating gate having a vertical length of less than

100 nanometers.

48. (Currently Amended) The electronic system of claim ~~44~~ 46, wherein the plurality of control gate lines are formed in the trench below the top surface of the pillar and between the pair of floating gates such that each trench houses a pair of control gate lines each addressing the floating gates one on opposing sides of the trench respectively, and wherein the pair of control gate lines are separated by an insulator layer.

49. (Currently Amended) The electronic system of claim ~~44~~ 46, wherein the plurality of control gate lines are disposed vertically above the floating gates, and wherein each pair of floating gates shares a single control gate line.

50. (Currently Amended) The electronic system of claim ~~44~~ 46, wherein the plurality of control gate lines are disposed vertically above the floating gates, and wherein each one of the pair of floating gates is addressed by an independent one of the plurality of control lines.

51. (Currently Amended) The electronic system of claim ~~40~~ 42, wherein each floating gate is a horizontally oriented floating gate formed in a trench below a top surface of each pillar such that each trench houses a floating gate opposing the body regions in adjacent pillars on opposing sides of the trench, and wherein each horizontally oriented floating gate has a vertical length of less than 100 nanometers opposing the body region of the pillars.

52. (Currently Amended) The electronic system of claim ~~49~~ 51, wherein the plurality of control gate lines are disposed vertically above the floating gates.

53. (Original) A method of forming a floating gate transistor, comprising:

forming a first source/drain region and a second source/drain region separated by a channel region in a substrate;

forming a floating gate opposing the channel region and separated therefrom by a gate oxide;

forming a control gate opposing the floating gate; and

forming a low tunnel barrier intergate insulator to separate the control gate from the floating gate.

54. (Currently Amended) The method of claim ~~51~~ 53, wherein forming the low tunnel barrier intergate insulator includes forming a metal oxide insulator selected from the group consisting of lead oxide (PbO) and aluminum oxide (Al_2O_3).

55. (Currently Amended) The method of claim ~~51~~ 53, wherein forming the low tunnel barrier intergate insulator includes forming a transition metal oxide insulator.

56. (Currently Amended) The method of claim ~~53~~ 55, wherein forming the transition metal oxide insulator includes forming the transition metal oxide insulator selected from the group consisting of Ta_2O_5, TiO_2, ZrO_2, and Nb_2O_5.

57. (Currently Amended) The method of claim ~~51~~ 53, wherein forming the floating gate includes forming a polysilicon floating gate having a metal layer formed thereon in contact with the low tunnel barrier intergate insulator.

58. (Currently Amended) The method of claim ~~51~~ 53, wherein forming the control gate includes a forming a polysilicon control gate having a metal layer formed thereon in contact with the low tunnel barrier intergate insulator.

59. (Original) A method for forming an array of flash memory cells, comprising:

forming a number of pillars extending outwardly from a substrate, wherein each pillar includes a first source/drain region, a body region, and a second source/drain region;

forming a number of floating gates opposing the body regions in the number of pillars and separated therefrom by a gate oxide;

forming a number of control gates opposing the floating gates;

forming a number of buried sourcelines disposed below the number of pillars and coupled

to the first source/drain regions along a first selected direction in the array of memory cells;

forming a number of control gate lines formed integrally with the number of control gates along a second selected direction in the array of flash memory cells, wherein the number of control gates lines are separated from the floating gates by a low tunnel barrier intergate insulator; and

forming a number of bitlines coupled to the second source/drain regions along a third selected direction in the array of flash cells.

60. (Currently Amended) The method of claim ~~57~~ 59, wherein forming the low tunnel barrier intergate insulator includes forming a metal oxide insulator selected from the group consisting of PbO, Al_2O_3, Ta_2O_5, TiO_2, ZrO_2, and Nb_2O_5.

61. (Currently Amended) The method of claim ~~57~~ 59, wherein forming each floating gate includes forming a polysilicon floating gate having a metal layer formed thereon in contact with the low tunnel barrier intergate insulator.

62. (Currently Amended) The method of claim ~~57~~ 59, wherein forming each control gate includes forming a polysilicon control gate having a metal layer formed thereon in contact with the low tunnel barrier intergate insulator.

63. (Currently Amended) The method of claim ~~57~~ 59, wherein forming each floating gate includes forming a vertical floating gate in a trench below a top surface of each pillar such that each trench houses a pair of floating gates opposing the body regions in adjacent pillars on opposing sides of the trench.

64. (Currently Amended) The method of claim ~~61~~ 63, wherein forming the plurality of control gate lines includes forming each control gate line in the trench below the top surface of the pillar and between the pair of floating gates, wherein each pair of floating gates shares a single control gate line, and wherein each floating gate includes a vertically oriented floating gate having a vertical length of less than 100 nanometers.

65. (Currently Amended) The method of claim ~~61~~ 63, wherein forming the plurality of control gate lines includes forming a pair of control gate lines in each trench below the top surface of the pillar and between the pair of floating gates such that each control gate line addresses a floating gate on opposing sides of the trench respectively, and wherein the pair of control gate lines are separated by an insulator layer.

66. (Currently Amended) The method of claim ~~61~~ 63, wherein forming the plurality of control gate lines includes forming the control gate lines such that the control gate lines are disposed vertically above the floating gates such that each pair of floating gates shares a single control gate line.

67. (Currently Amended) The method of claim ~~61~~ 63, wherein forming the plurality of control gate lines includes forming the control gate lines such that the control gate lines are disposed vertically above the floating gates, and forming the plurality of control lines such that each one of the pair of floating gates is addressed by an independent one of the plurality of control lines.

68. (Currently Amended) The method of claim ~~57~~ 59, wherein forming each floating gate includes forming a horizontally oriented floating gate in a trench below a top surface of each pillar such that each trench houses a floating gate opposing the body regions in adjacent pillars on opposite sides of the trench, and wherein each horizontally oriented floating gate has a vertical length of less than 100 nanometers opposing the body region of the pillars.

69. (Currently Amended) The method of claim ~~66~~ 68, wherein the forming the plurality of control gate lines includes forming the control gate lines such that the control gate lines are disposed vertically above the floating gates.

70. (Original) A method for operating a non-volatile memory cell, comprising:
writing to a floating gate of the non-volatile memory cell using channel hot electron

injection, wherein the non–volatile memory cell includes:

a first source/drain region and a second source/drain region separated by a channel region in a substrate;

a floating gate opposing the channel region and separated therefrom by a gate oxide;

a control gate opposing the floating gate; and

wherein the control gate is separated from the floating gate by a low tunnel barrier intergate insulator;

erasing charge from the floating gate by tunneling electrons off of the floating gate and onto the control gate.

71. (Currently Amended) The method of claim ~~68~~ 70, wherein erasing charge from the floating gate by tunneling electrons off of the floating gate and onto the control gate further includes:

providing a negative voltage to the substrate; and

providing a large positive voltage to the control gate.

72. (Currently Amended) The method of claim ~~68~~ 70, wherein the method further includes writing to the floating gate by tunneling electrons from the control gate to the floating gate.

73. (Currently Amended) The method of claim ~~69~~ 72, wherein writing to the floating gate by tunneling electrons from the control gate to the floating gate further includes:

applying a positive voltage to the substrate; and

applying a large negative voltage to the control gate.

74. (Currently Amended) The method of claim ~~69~~ 72, wherein erasing charge from the floating gate by tunneling electrons off of the floating gate and onto the control gate includes tunneling electrons from the floating gate to the control gate through a low tunnel barrier intergate insulator.

75. (Currently Amended) The method of claim ~~72~~ 74, wherein tunneling electrons from the floating gate to the control gate through a low tunnel barrier intergate insulator includes tunneling electrons from the floating gate to the control gate through a low tunnel barrier intergate insulator selected from the group consisting of PbO, Al_2O_3, Ta_2O_5, TiO_2, ZrO_2, and Nb_2O_5.

76. (Currently Amended) The method of claim ~~72~~ 74, wherein tunneling electrons from the floating gate to the control gate through a low tunnel barrier intergate insulator includes tunneling electrons from a metal layer formed on the floating gate in contact with the low tunnel barrier intergate insulator to a metal layer formed on the control gate and also in contact with the low tunnel barrier intergate insulator.

77. (Original) A method for operating an array of flash memory cells, comprising:

writing to one or more floating gates for a number of non-volatile memory cells in the array of flash memory cells using channel hot electron injection, the array of flash memory cells includes:

a number of pillars extending outwardly from a substrate, wherein each pillar includes a first source/drain region, a body region, and a second source/drain region;

a number of floating gates opposing the body regions in the number of pillars and separated therefrom by a gate oxide;

a number of control gates opposing the floating gates;

a number of buried sourcelines disposed below the number of pillars and coupled to the first source/drain regions along a first selected direction in the array of memory cells;

a number of control gate lines formed integrally with the number of control gates along a second selected direction in the array of flash memory cells, wherein the number of control gates lines are separated from the floating gates by a low tunnel barrier intergate insulator; and

a number of bitlines coupled to the second source/drain regions along a third selected direction in the array of flash cells; and

erasing charge from the one or more floating gates by tunneling electrons off of the one or more floating gates and onto the number of control gates.

78. (Currently Amended) The method of claim ~~75~~ 77, wherein erasing charge from the one or more floating gates by tunneling electrons off of the floating gate and onto the number of control gate further includes:

providing a negative voltage to a substrate of one or more non-volatile memory cells; and

providing a large positive voltage to the control gate for the one or more non-volatile memory cells.

79. (Currently Amended) The method of claim ~~76~~ 78, wherein the method further includes erasing an entire row of non-volatile memory cells by providing a negative voltage to all of the substrates along an entire row of non-volatile memory cells and providing a large positive voltage to all of the control gates along the entire row of non-volatile memory cells.

80. (Currently Amended) The method of claim ~~76~~ 78, wherein the method further includes erasing an entire block of non-volatile memory cells by providing a negative voltage to all of the substrates along multiple rows of non-volatile memory cells and providing a large positive voltage to all of the control gates along the multiple rows of non-volatile memory cells.